

# Aion Attacks: Exposing Software Timer Problem in Trusted Execution Environment

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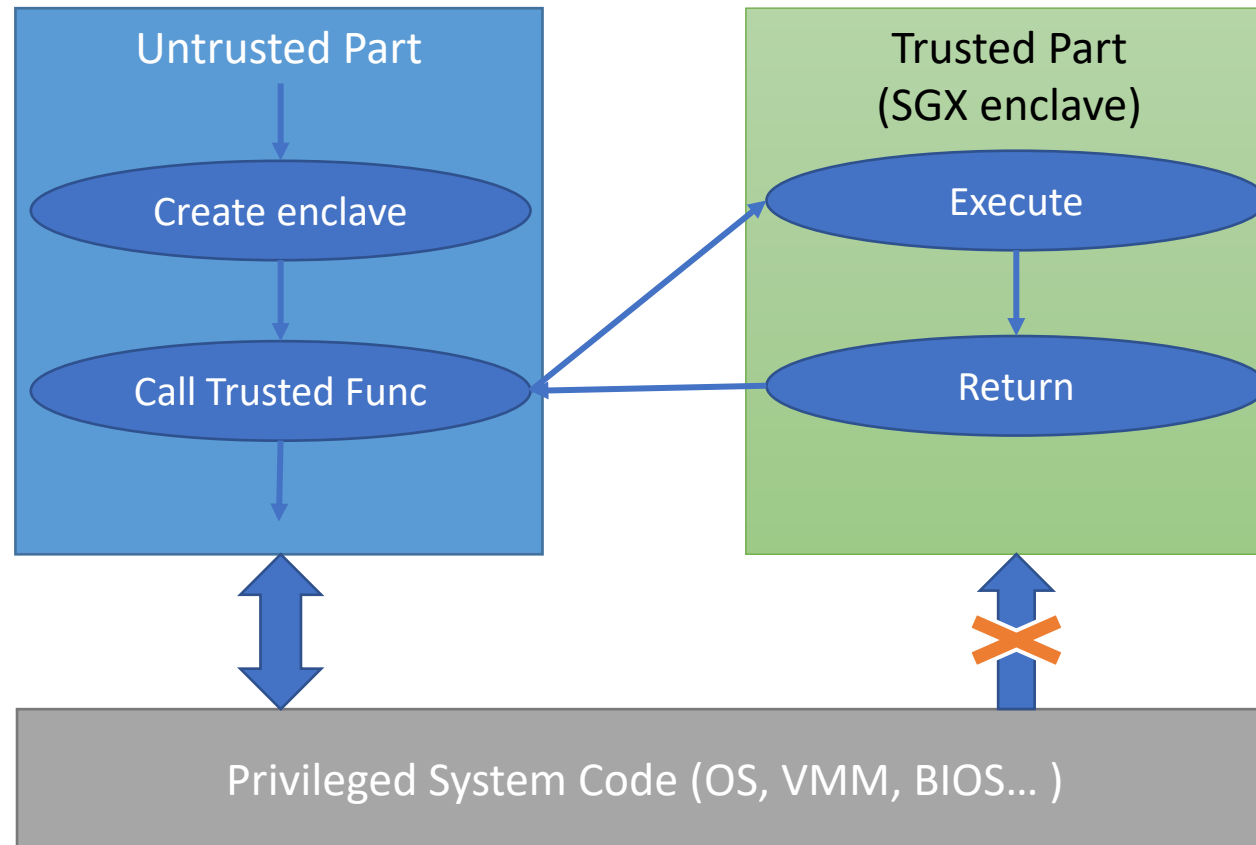
<sup>2</sup> NIO



# Outline

- Introduction and Background
- SGX Defence and Issues
- Software Timer Model
- Attack Design
- Evaluation
- Conclusion

# Background of Intel SGX



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- Side-channel vulnerabilities
- Cache-channel attack

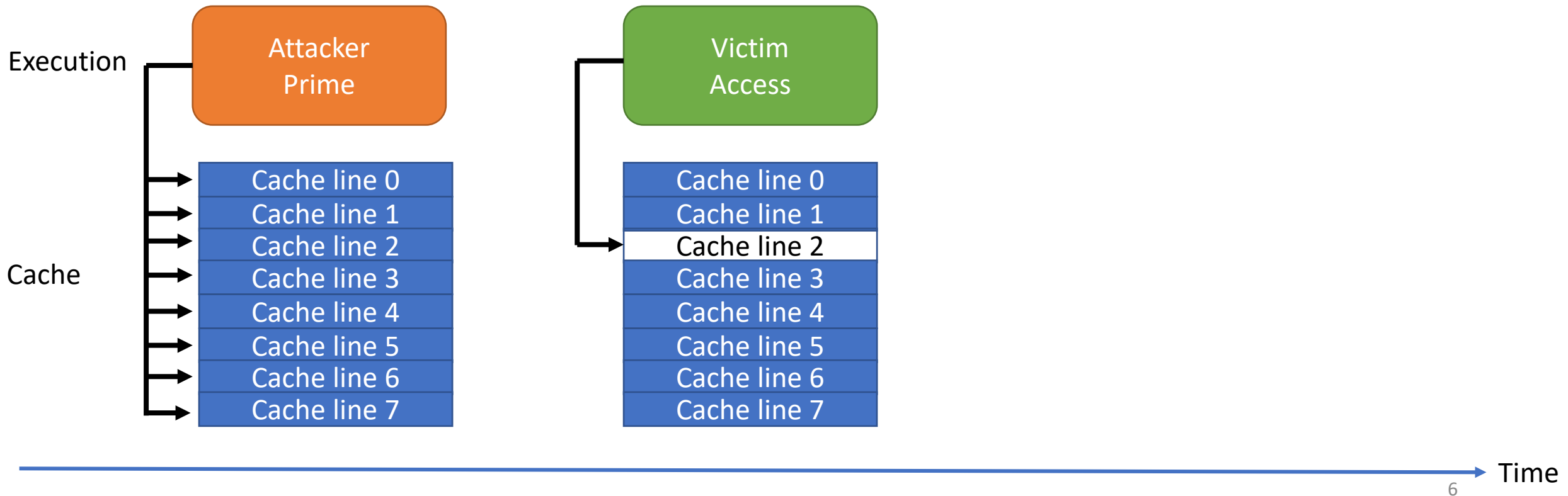
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- Side-channel vulnerabilities
- Cache-channel attack



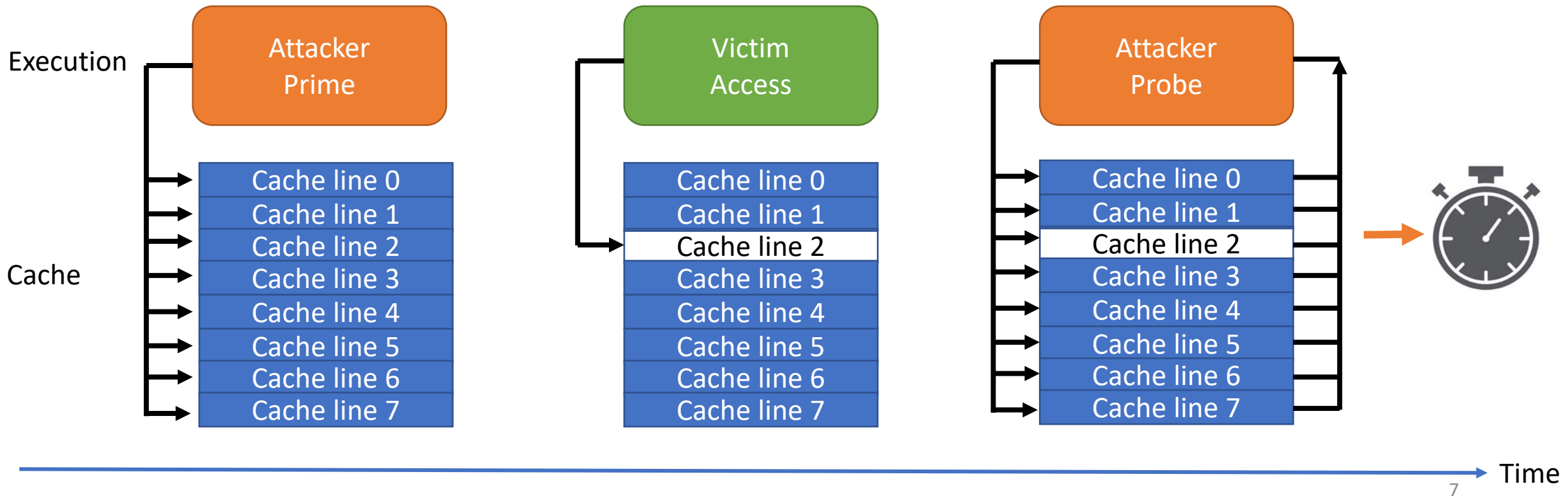
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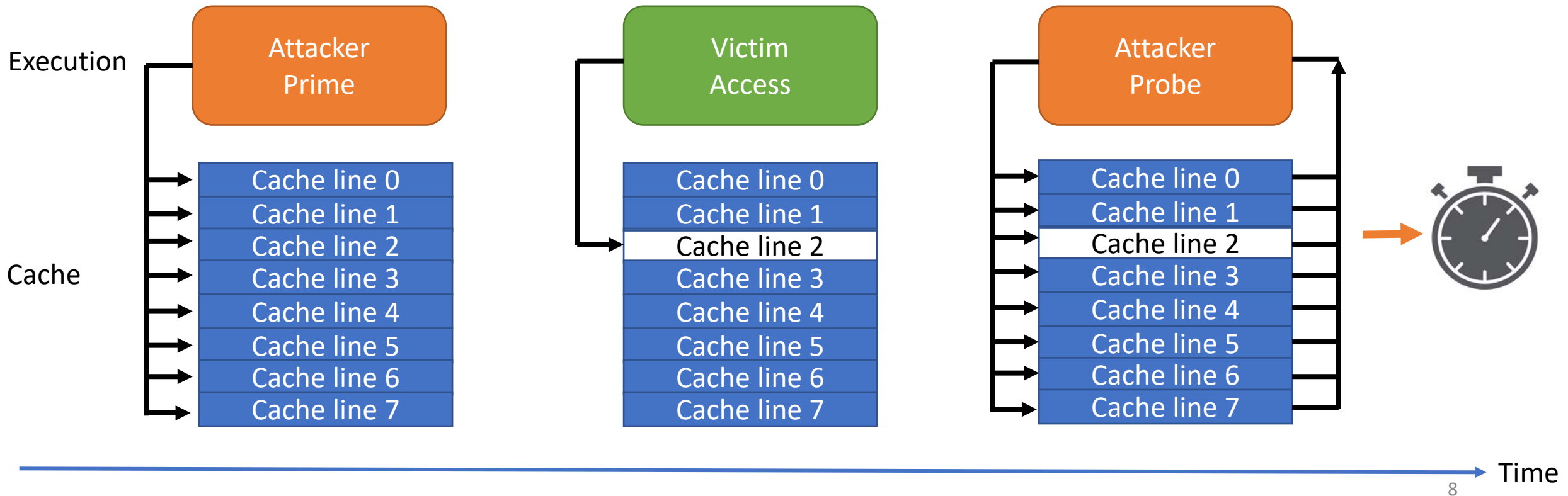
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# Background of Intel SGX

- Side-channel vulnerabilities
- Cache-channel attack
  - Attacking thread shares cache with victim
  - Proper timing of Prime and Probe
  - Timing all cache lines





# SGX Defender Review

- Defending SGX side-channel attacks
  - Software developers' job

[Intel SDM]

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- Defenders need high-resolution timers:
  - To count the time interval of certain events
    - Period of time before another enclave interrupt
    - Compare against baseline during calibration

[Intel SDM]

[Déjà Vu'17]

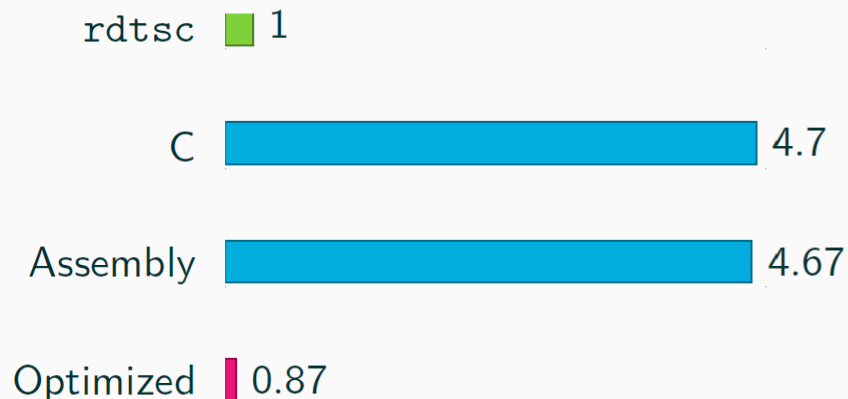
# SGX Defender Review

- Defending SGX side-channel attacks
  - Software developers' job [Intel SDM]
- Defenders need high-resolution timers:
  - To count the frequency of abnormal behaviors [Déjà Vu'17]
    - Number of interrupts to victim enclave
    - Compare against baseline during calibration
  - To determine if two threads are co-located [Varys'19]
    - On the same physical core, share L2 cache
    - Compare access time of same variable, L2 normally  $\sim 10$  cycles

# SGX defence review

- No hardware timer available in SGX
- Importance of an accurate software timer
  - Set a baseline of how much time an event takes
  - Decide how often suspicious behaviors happen
- Challenge: granularity of timer

CPU cycles one increment takes

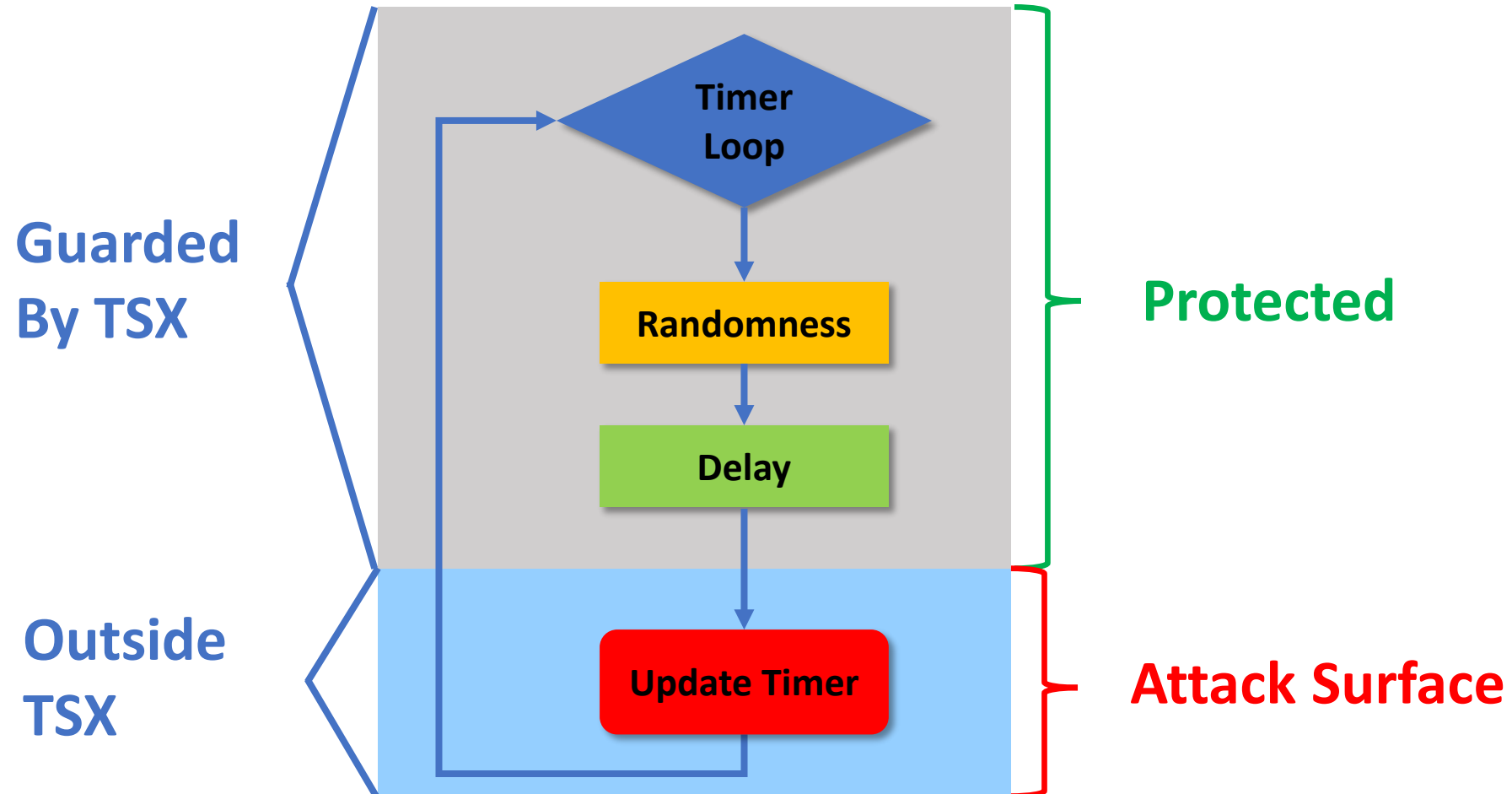


```
1 mov &timestamp, %rcx
2 1: inc %rax
3 mov %rax, (%rcx)
4 jmp 1b
```

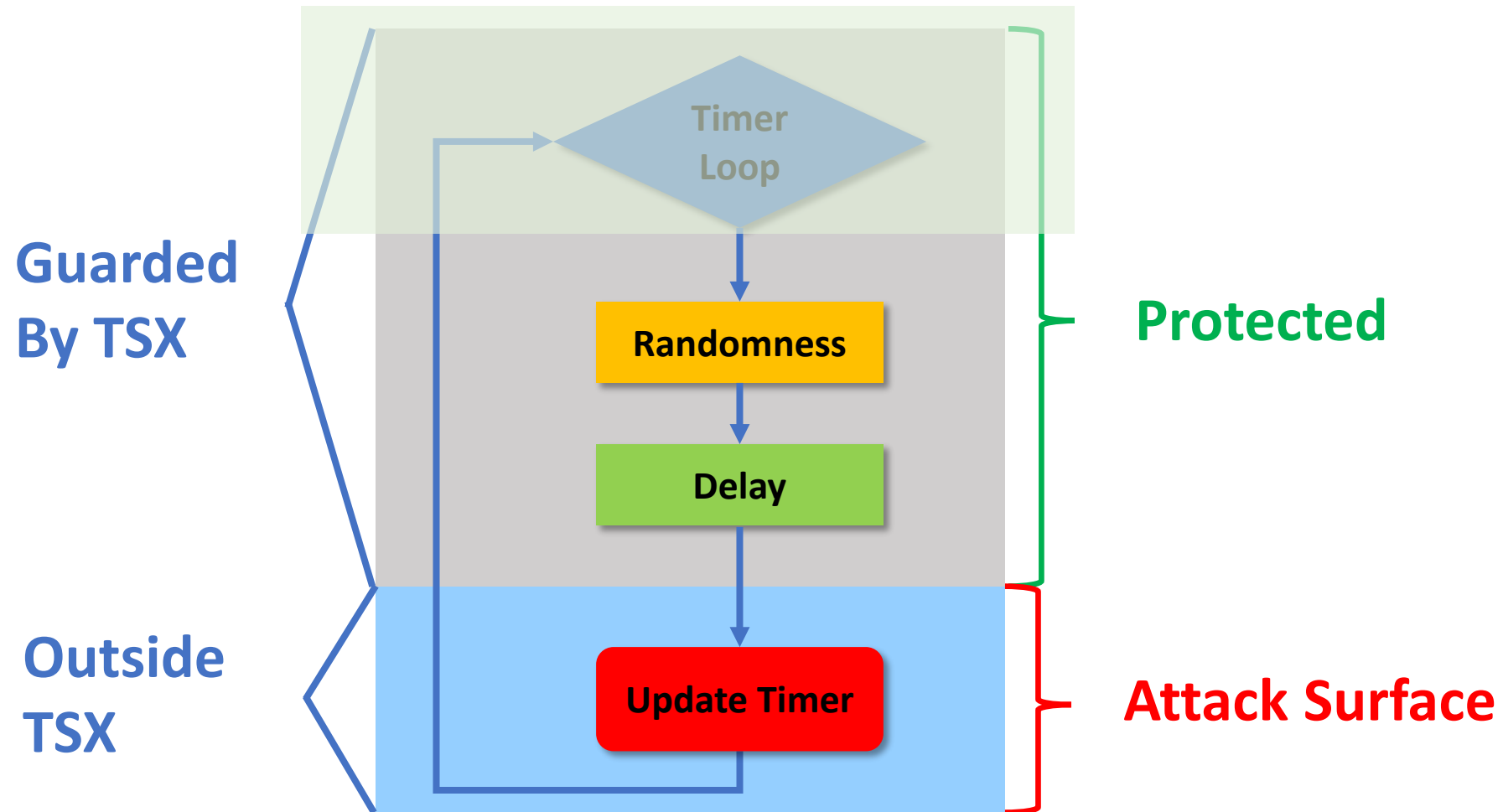
```
1 while (1) {
2   timestamp++;
3 }
```

DRAM/Cache  
Access

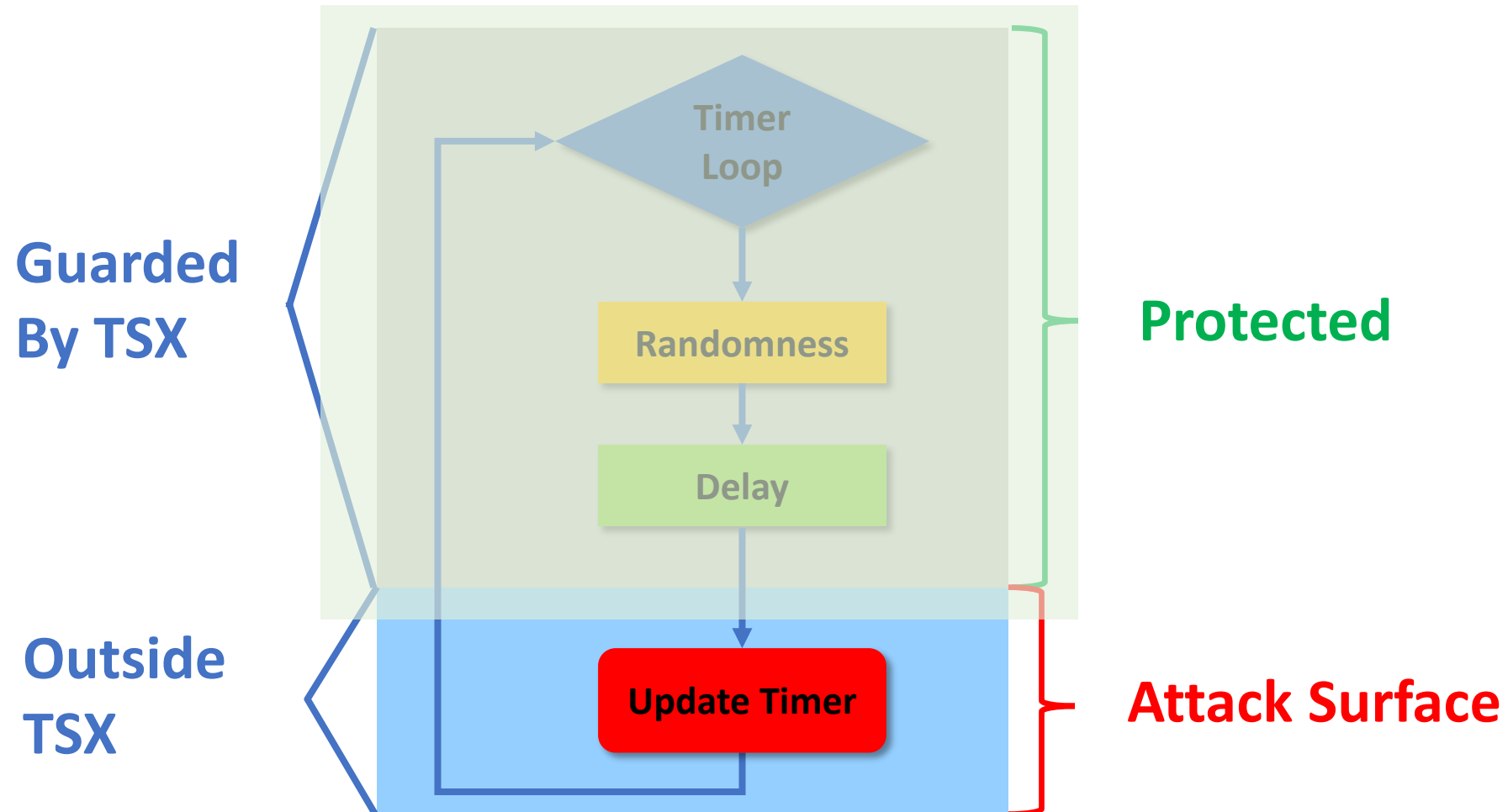
# Software Timer Modeling



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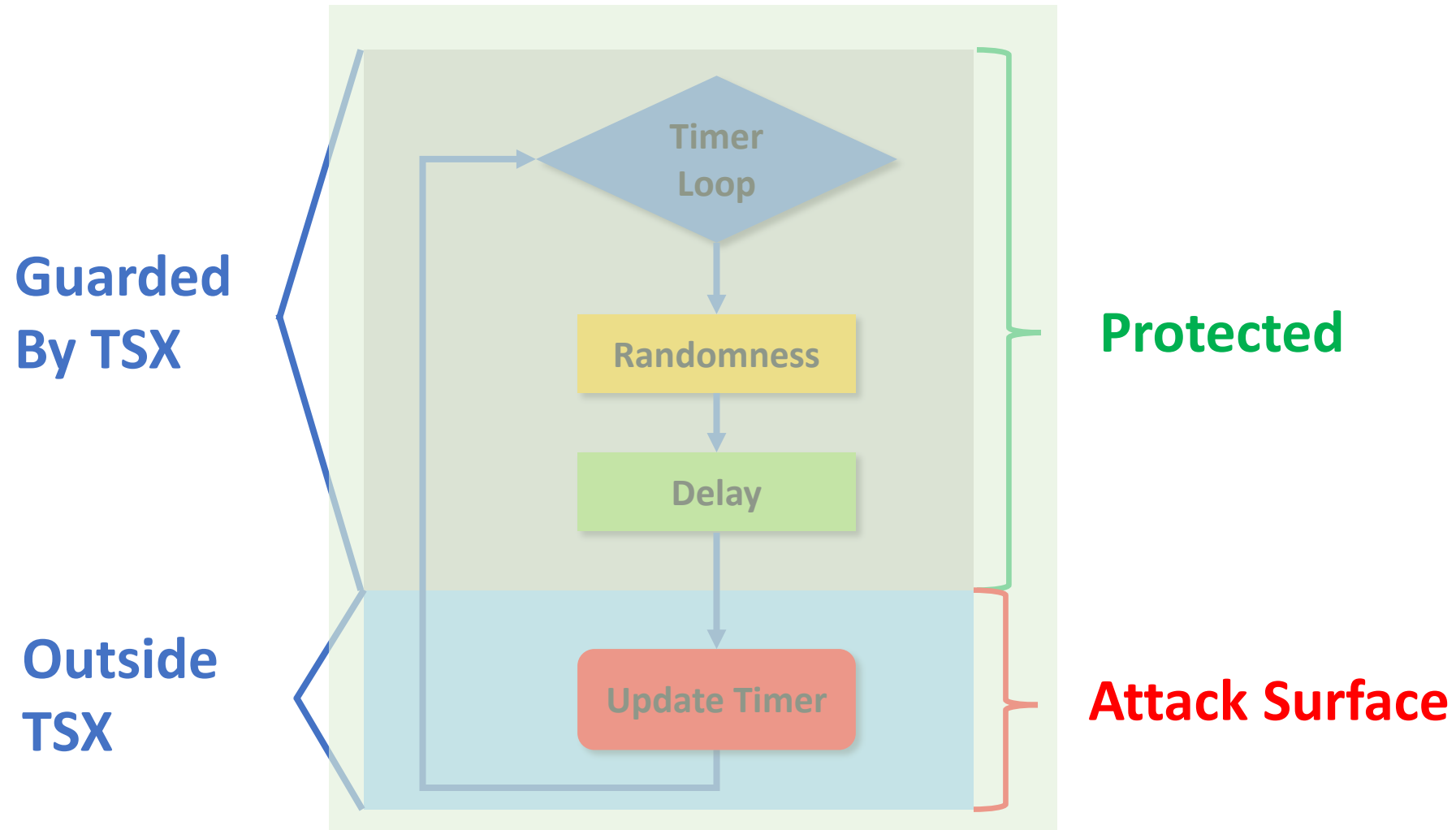


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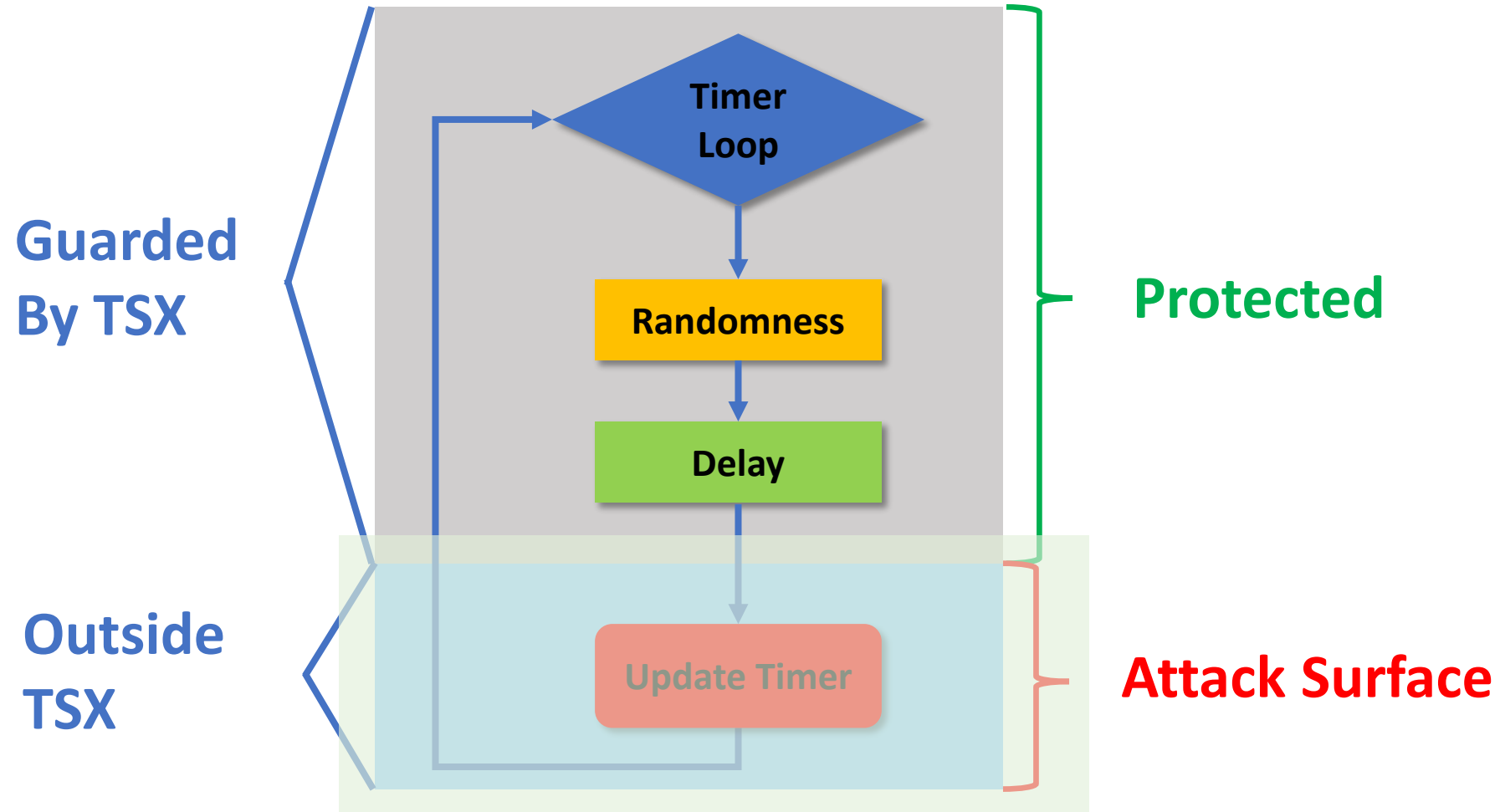




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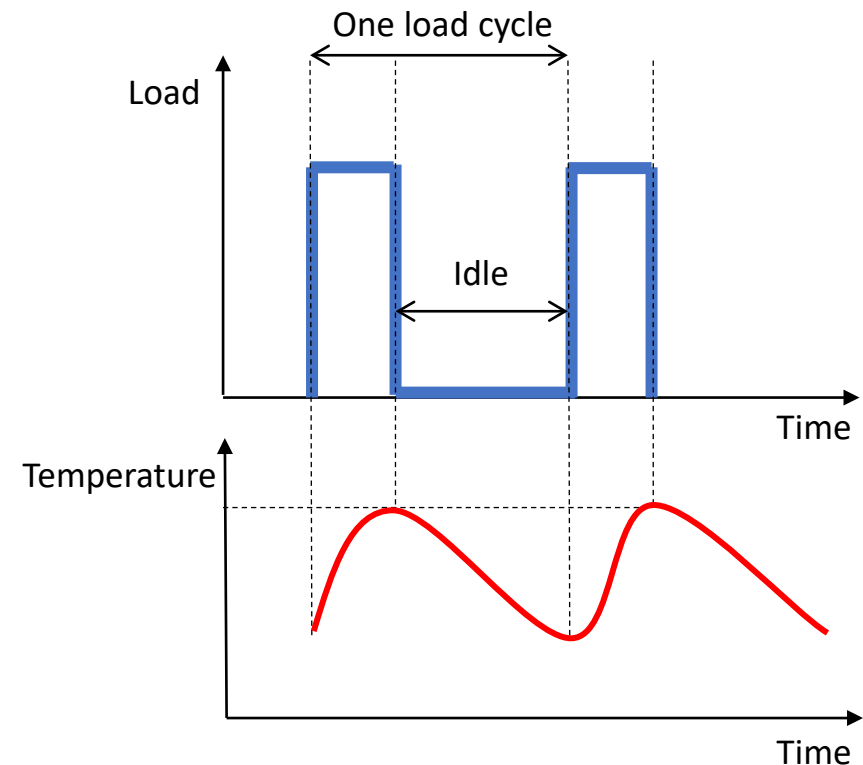


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- Intel Processors:
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    - Software-adjustable Thermal activation offset
    - Slow down target cores when triggered

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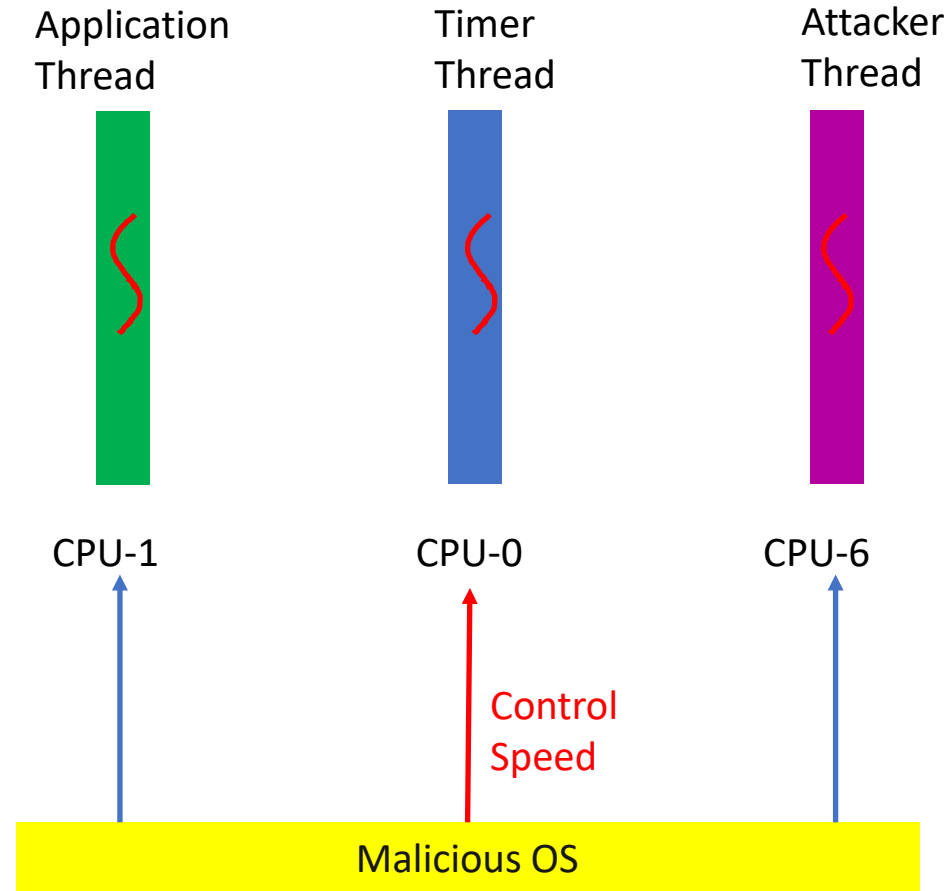
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  - HDC
    - MSRs to control hardware duty cycling
    - Per-core control, works with hyper-threading
    - Slow down target threads by more than 20x



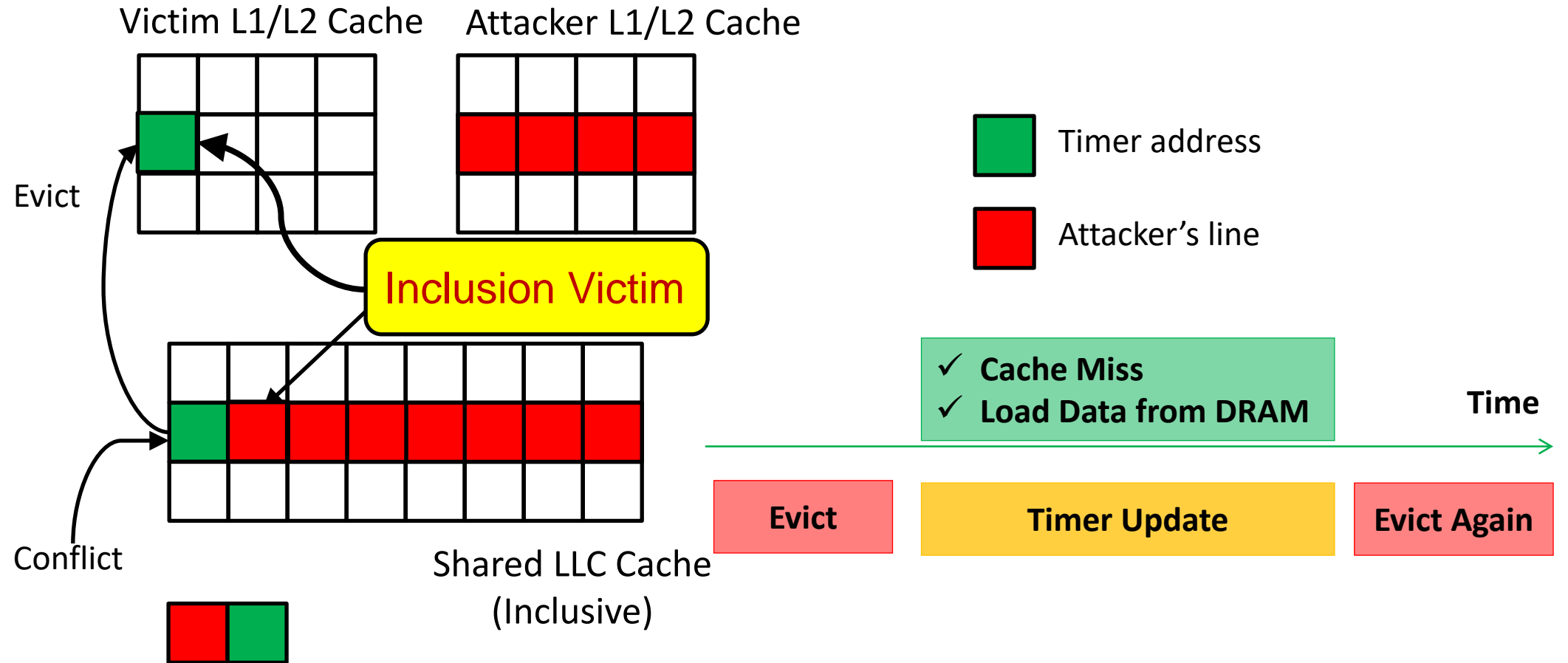
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- Other processors
  - Similar mechanisms
    - AMD: Hardware Thermal Control, P-state MSRs

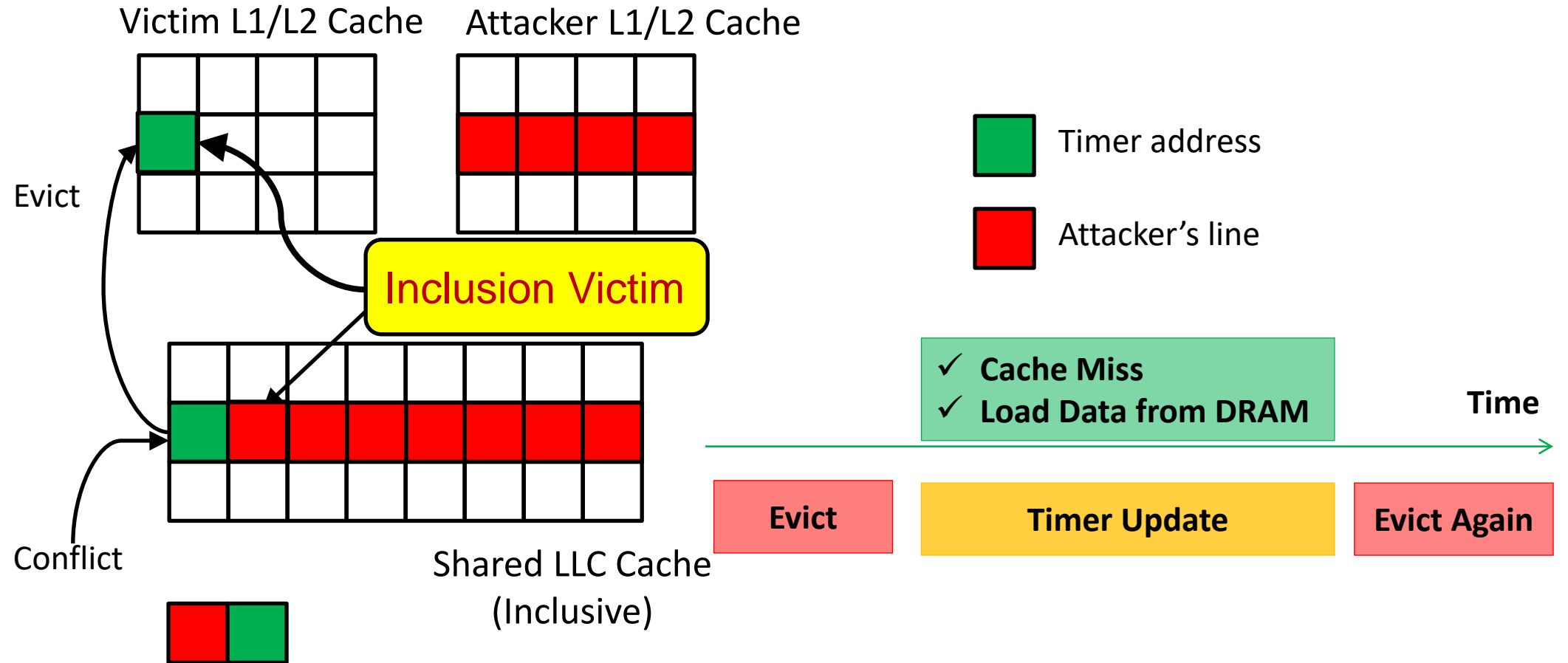
# Aion Attacks: Thermal Attack



# Aion Attacks: Eviction Attack



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# Evaluation Results

- Software timer to measure the same piece of code
- Attackers try to slow down the software timer

	Xeon E3-1230v6		i7-6700K	
	RNG-1	RNG-2	RNG-1	RNG-2
<b>Baseline time (s)</b>	256.3	337.4	225.9	302.5
<b>Eviction Attack</b>	1.6x	1.9x	1.5x	2.0x
<b>Multi-thread Eviction Attack</b>	2.7x	6.2x	2.5x	7.3x
<b>Multi-thread Eviction + Thermal Attack</b>	111x	187x	120x	202x

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- Aion attack to help other side-channel attacks evade detection

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	Threshold	Acc %	False-Positive %	Threshold	Acc % (E3)	Acc % (i7)
Numeric sort	4	100	97	4	95	94
	40	100	40	40	17	15
	<b>80</b>	<b>95</b>	<b>3</b>	<b>80</b>	<b>2</b>	<b>2</b>
	160	87	2	160	1	0
	320	40	0	320	0	0
	640	9	0	-	-	-
	1280	3	0	-	-	-
Fourier	4	100	98	4	95	92
	40	100	46	40	19	18
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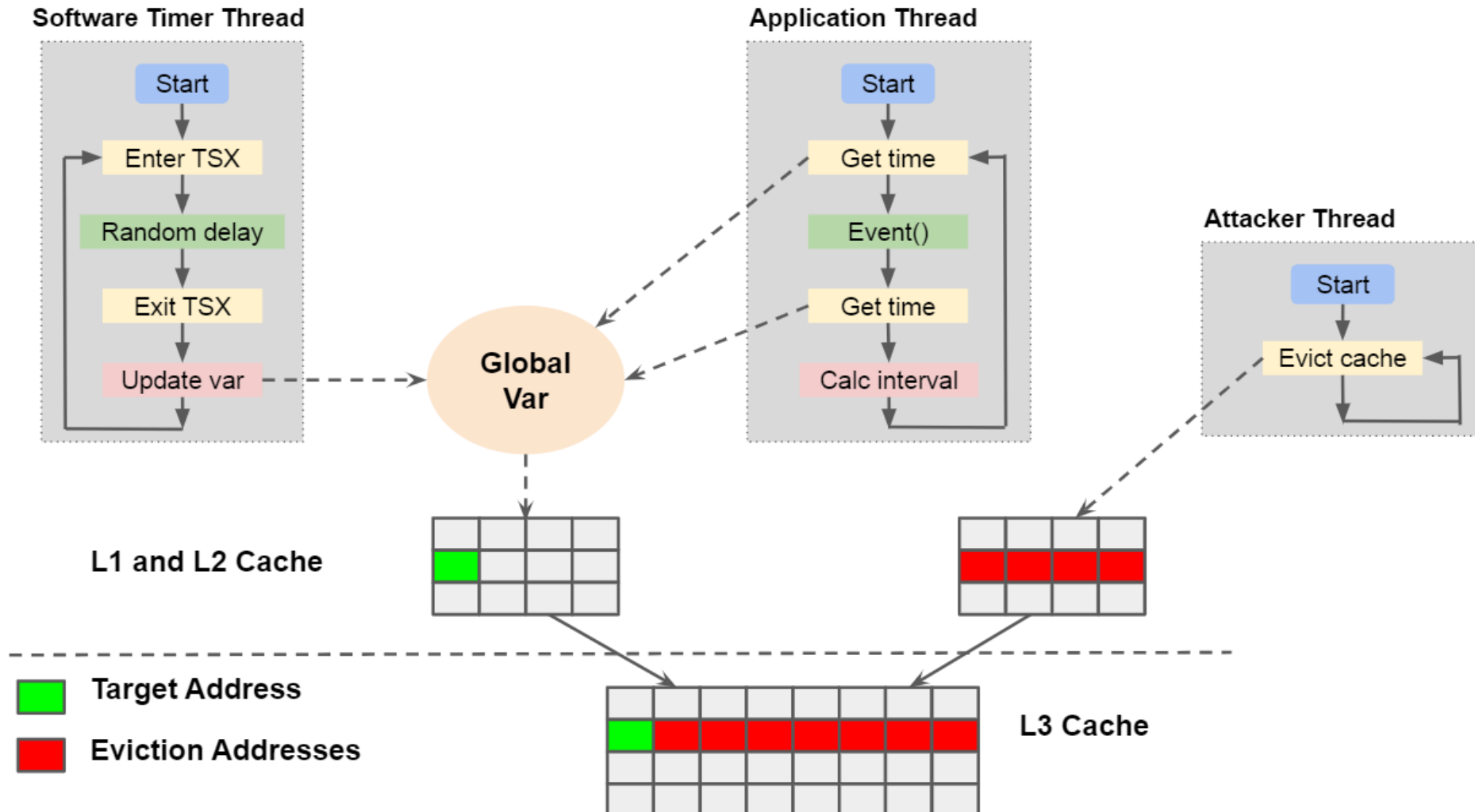
# Conclusion and Discussions

- Software timer will always be unreliable
- Better seek hardware assistance
- What about SGX 2.0?

# Q&A

- Thanks!

# Back-up Slide 1: Eviction algorithm



# Back-up Slide 2: Cache slices

